| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/777,156 | MAYAMA ET AL. | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/20/05*.

2. ☒ The allowed claim(s) is/are *1 - 6, 9 - 12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Supplemental Amendment*.

## REASONS FOR ALLOWANCE

Examiner acknowledges a submission of the amendment and arguments filed on September 20, 2005 and Supplemental Amendment on November 7, 2005. Amendment and arguments have overcome rejections under 103(a).

The following is an examiner's statement of reasons for allowance:
An amended independent Claim 1 discloses a protection circuit, to be provided for a circuit arrangement having an inductive load and an FET as an N-channel MOS transistor provided upstream of the load with respect to a flow of power current, the FET controlling an energization state of the load, the protection circuit comprising: a first connection changer interposed on a connection line between a gate of the FET and a gate drive voltage supply source, the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground; and a first resistor interposed between the gate and a source of the FET, wherein the protection circuit does not include a zener diode, and protects from overvoltage regenerated by the load upon discontinuing power to the load.

The closest reference for the claim is Izawa et al., which discloses following elements: an FET as an N-channel MOS transistor (element 18 in Fig. 2) provided upstream of the load with respect to a flow of power current, the FET controlling an activation state of the load, the protection circuit including: a first connection changer

(element 20 in Fig. 2) interposed on a connection line between a gate of the FET and a gate drive voltage supply source (elements 15 and 16 in Fig. 2), the first connection changer changing a connection state between a first connection state in which the gate is connected to the gate drive voltage supply and a second connection state in which the gate is connected to a ground (col. 14, line 65 24 – col. 15, line13); the first connection line connects a gate of the FET and a gate drive voltage supply source.

However, the Izawa reference (I) is not concerned with protection of the FET from overvoltage generated by the load upon discontinuing power to the load and (II) it does not disclose the resistor connected between a gate and a source of the transistor.

The closest second reference is Tabata et al. (US 4,914,540), which discloses the overvoltage protection device (shown in Fig. 4) having the FET protected from overvoltage stress by a voltage divider with one of the resistors connected between the gate and the source of the FET. However, (I) addition of the voltage divider according to the Izawa circuit would be impossible since the FET in Izawa circuit has a gate coupled to the charge pump and level shifter connected to the gate and the gate is normally maintained at the potential higher than the power supply (Vb in Fig. 2), therefore the voltage divider of Tabata et al. will interfere with the level shifter activity, and (II) the Izawa circuit is designed with the goals of the thermal and overcurrent protection, two tasks, which are schematically complementary, while protection from overvoltage generated by the downstream load is totally foreign to the Izawa circuit and there is no motivation to modify the circuit in such way.

The limitation of the overvoltage protection and presence of the gate to source resistor is recited over again in other independent claims 4, 9 and 11, thus making them allowable.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
11/8/2005

BRIAN SIRCUS
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